Frequency Synthesizers for RF Transceivers
Modelling of PLL in the frequency and time domain with a design example

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Outline

1. CP-PLL models
   - The need for accurate PLL models
   - s-domain model
   - z-domain model
   - Time-domain model
   - Comparison between models
   - Phase Noise Models

2. Design Example: Frequency Synthesizer for UWB MB-OFDM
   - UWB communications
   - Synthesizer Architecture
   - PLLs
   - Tuning Range Extension
   - Measured results
Outline

1. CP-PLL models
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     - s-domain model
     - z-domain model
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   - Measured results
**Charge Pump Phase Locked Loops (CP-PLLs)**

Charge Pump Phase Locked Loop

- **PFD-CP** compares phase misalignment between feedback and reference signal.
- Loop Filter integrates error signal and controls VCO output frequency.
- When in-lock, $F_{OUT} = N \cdot F_{REF}$.
- Loop tracks phase and frequency misalignments with zero errors.
Charge Pump Phase Locked Loops (CP-PLLs)

Charge Pump Phase Locked Loop

- CP, LF and VCO are continuous-time systems.
- PFD and FD are edge-driven systems.
- Phase comparison is performed once per reference period, not continuously.
The need for accurate PLL models

Simulations need to be performed hierarchically. Circuit level time-domain simulation is not feasible.
The need for accurate PLL models

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The need for accurate PLL models

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Traditional models (*s-domain and z-domain*) rely on linearizations and approximations to simplify loop analysis.

Efficient semi-analytical time-domain models can avoid these approximations, with reduced computation time.
The need for accurate PLL models

PLL models

- Simulations need to be performed hierarchically. Circuit level time-domain simulation is not feasible.
- Traditional models (*s-domain and z-domain*) rely on linearizations and approximations to simplify loop analysis.
- Efficient semi-analytical time-domain models can avoid these approximations, with reduced computation time.
- Derivation and comparison between these models is performed.
Outline

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Fourth order PLL s-domain model

Approximation

Charge injected by charge pump over one period:

\[ Q = \frac{\theta_r - \theta_d}{2\pi} GT \]
Fourth order PLL s-domain model

Approximation

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- If the loop dynamic is *slow enough* one can neglect the CP current actual shape.
Approximation

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  \[ Q = \frac{\theta_r - \theta_d}{2\pi} GT \]

- If the loop dynamic is slow enough one can neglect the CP current actual shape

- and substitute it with an average current: 
  \[ i_{CP} = G\frac{\theta_r - \theta_d}{2\pi} \]
Fourth order PLL s-domain model

Approximation

- Charge injected by charge pump over one period:
  \[ Q = \frac{\theta_r - \theta_d}{2\pi} GT \]

- If the loop dynamic is *slow enough* one can neglect the CP current actual shape

- and substitute it with an average current:
  \[ i_{CP} = G\frac{\theta_r - \theta_d}{2\pi} \]

- Averaged linear continuous time PLL model
s-domain model transfer functions

CP-PFD

\[ i_{CP} = G \frac{\theta_r - \theta_d}{2\pi} \rightarrow \frac{i_{CP}(s)}{\theta_r(s) - \theta_d(s)} = \frac{G}{2\pi} \]
s-domain model transfer functions

**CP-PFD**

\[ i_{CP} = G \frac{\theta_r - \theta_d}{2\pi} \rightarrow \frac{l_{CP}(s)}{\theta_r(s) - \theta_d(s)} = \frac{G}{2\pi} \]

**3rd order LF**

\[ G_{LF}(s) = \frac{V_{C}(s)}{I_{CP}(s)} = \frac{K_{LF}}{s + 1/\tau_z} \frac{s + b/\tau_z}{s(c/\tau_z)} \]
s-domain model transfer functions

**CP-PFD**

\[
\begin{align*}
    i_{CP} &= G \frac{\theta_r - \theta_d}{2\pi} \\
    \frac{l_{CP}(s)}{\theta_r(s) - \theta_d(s)} &= \frac{G}{2\pi}
\end{align*}
\]

**3rd order LF**

\[
G_{LF}(s) = \frac{V_C(s)}{I_{CP}(s)} = K_{LF} \frac{s + 1/\tau_z}{s \cdot (s + b/\tau_z) \cdot (s + c/\tau_z)}
\]

**QVCO**

\[
\begin{align*}
    f_o &= K_{VCO} \cdot V_C, \quad \theta_o = \int 2\pi f_o(t) dt \\
    \frac{\theta_o(s)}{V_C(s)} &= \frac{2\pi \cdot K_{VCO}}{s}
\end{align*}
\]
s-domain model transfer functions

**CP-PFD**

\[ i_{CP} = G \theta_r - \theta_d \frac{2\pi}{2\pi} \rightarrow \frac{l_{CP}(s)}{\theta_r(s) - \theta_d(s)} = \frac{G}{2\pi} \]

**3rd order LF**

\[ G_{LF}(s) = \frac{V_C(s)}{I_{CP}(s)} = \frac{s + 1/\tau_z}{K_{LF} \cdot s \cdot (s + b/\tau_z) \cdot (s + c/\tau_z)} \]

**QVCO**

\[ f_o = K_{VCO} \cdot V_C, \theta_o = \int 2\pi f_o(t)dt \]

\[ \frac{\theta_o(s)}{V_C(s)} = \frac{2\pi \cdot K_{VCO}}{s} \]

**FD**

\[ \frac{\theta_d(s)}{\theta_o(s)} = \frac{1}{N} \]
Fourth order PLL s-domain model

Open loop transfer function...

\[ G_c(s) = \frac{G \cdot K_{VCO} \cdot G_{LF}(s)}{s \cdot N} \]
Fourth order PLL s-domain model

Open loop transfer function...

\[ G_c(s) = \frac{G \cdot K_{VCO} \cdot G_{LF}(s)}{s \cdot N} \]

... for third order LF...

\[ G_c(s) = K_C \frac{s + 1/\tau_z}{s^2 \cdot (s + b/\tau_z) \cdot (s + c/\tau_z)} \]
Fourth order PLL s-domain model

Open loop transfer function...

$$G_c(s) = \frac{G \cdot K_{VCO} \cdot G_{LF}(s)}{s \cdot N}$$

... for third order LF...

$$G_c(s) = K_C \frac{s + 1/\tau_z}{s^2 \cdot (s + b/\tau_z) \cdot (s + c/\tau_z)}$$

... with

$$K_C = \frac{GK_{VCO}K_{LF}}{N}.$$
Fourth order PLL s-domain model

Open loop transfer function...

\[ G_c(s) = \frac{G \cdot K_{VCO} \cdot G_{LF}(s)}{s \cdot N} \]

Closed loop transfer function

\[ \frac{\theta_o}{\theta_r} = \frac{G \cdot K_{VCO}N \cdot G_{LF}(s)}{s \cdot N + G \cdot K_{VCO} \cdot G_{LF}(s)} \]

... for third order LF...

\[ G_c(s) = K_C \frac{s + 1/\tau_z}{s^2 \cdot (s + b/\tau_z) \cdot (s + c/\tau_z)} \]

... with

\[ K_C = \frac{G K_{VCO} K_{LF}}{N}. \]
Fourth order PLL s-domain model

Open loop transfer function...

\[
G_c(s) = G_c \cdot K_{VCO} \cdot G_LF(s)
\]

Closed loop transfer function

\[
\theta_o = G_c \cdot K_{VCO} \cdot N \cdot G_LF(s) - G_c \cdot K_{VCO} \cdot G_LF(s)
\]

... for third order LF...

\[
G_c(s) = K_C \left( \frac{s + 1/\tau_z}{s^2 \cdot (s + b/\tau_z) \cdot (s + c/\tau_z)} \right)
\]

... with

\[
K_C = \frac{G K_{VCO} K_LF}{N}
\]
Fourth order PLL s-domain model

Open loop transfer function...

\[ G_c(s) = K_C \frac{s + 1/\tau_z}{s^2 \cdot (s + b/\tau_z) \cdot (s + c/\tau_z)} \]

Closed loop transfer function

\[ \theta_o \]

Rule of thumb for design

\[ f_c = \frac{1}{t_{lock} \cdot \zeta_e (\phi_m)} \ln \left( \frac{f_{step}}{f_{error}} \right) \]
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Fourth order PLL z-domain model

PFD granularity effects when the loop bandwidth is too large.

- Compute z-domain model by
  1. Substitute to the real CP input, weighted impulses of same area as the real pulse.
  2. Compute open loop impulse response $g_c(t)$ antitransforming $G_C(s)$.
  3. Sample the obtained equation every $T$.
  4. Z-transform to obtain $G_D(z)$.
  5. Compute closed-loop transfer function from $G_D(z)$. 
Z-domain model

Antittransform open loop transfer function

\[ G_C(s) = K_C \left[ \frac{As + B}{s^2} + \frac{C}{s + \frac{b}{\tau_z}} + \frac{D}{s + \frac{c}{\tau_z}} \right] \]
Z-domain model

**Antitransform open loop transfer function**

\[ G_C(s) = K_C \left[ \frac{As + B}{s^2} + \frac{C}{s + \frac{b}{\tau_z}} + \frac{D}{s + \frac{c}{\tau_z}} \right] \]

**Impulse response**

\[ g_c(t) = K_C[Au(t) + Bt + Ce^{-\frac{bt}{\tau_z}} + De^{-\frac{ct}{\tau_z}}] \]
Z-domain model

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**Impulse response**

\[ g_c(t) = K_C[Au(t) + Bt + Ce^{-\frac{bt}{\tau_z}} + De^{-\frac{ct}{\tau_z}}] \]

**Sampled impulse response**

\[ g_d(n) = K_C[Au(nT) + BnT + Ce^{-\frac{bnT}{\tau_z}} + De^{-\frac{cnT}{\tau_z}}] \]
Z-domain model

**Antitransform open loop transfer function**

\[
G_C(s) = K_C \left[ \frac{As + B}{s^2} + \frac{C}{s + \frac{b}{\tau_z}} + \frac{D}{s + \frac{c}{\tau_z}} \right]
\]

**Impulse response**

\[
g_c(t) = K_C [Au(t) + Bt + Ce^{-\frac{bt}{\tau_z}} + De^{-\frac{ct}{\tau_z}}]
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**Sampled impulse response**

\[
g_d(n) = K_C [Au(nT) + BnT + Ce^{-\frac{bnT}{\tau_z}} + De^{-\frac{cnT}{\tau_z}}]
\]

**z-Transform**

\[
G_D(z) = \left[ \frac{K_C TAz}{z - 1} + \frac{K_C BT^2 z}{(z - 1)^2} + \frac{K_C TCz}{z - e^{-\frac{bt}{\tau_z}}} + \frac{K_C TDz}{z - e^{-\frac{ct}{\tau_z}}} \right]
\]
Closed loop transfer function

\[ T_D(z) = \frac{\theta_o(z)}{\theta_i(z)} = \frac{N \cdot G_D(z)}{1 + G_D(z)} \]
Z-domain model - Step five

Closed loop transfer function

\[ T_D(z) = \frac{\theta_o(z)}{\theta_i(z)} = \frac{N \cdot G_D(z)}{1 + G_D(z)} \]

Antitransforming

\[ \theta_o(n) = \sum_{i=1}^{4} h_u(i) \cdot \theta_o(n - i) + \sum_{i=1}^{3} h_v(i) \cdot \theta_i(n - i) \]
Z-domain model - Step five

Closed loop transfer function

\[ T_D(z) = \frac{\theta_o(z)}{\theta_i(z)} = \frac{N \cdot G_D(z)}{1 + G_D(z)} \]

Antitransforming

\[ \theta_o(n) = \sum_{i=1}^{4} h_u(i) \cdot \theta_o(n-i) + \sum_{i=1}^{3} h_v(i) \cdot \theta_i(n-i) \]

With

\[
\begin{align*}
    h_u(1) &= \beta + \gamma + 2 + A'(\beta + \gamma + 1) - B' T + C'(\gamma + 2) + D'(\beta + 2) \\
    h_u(2) &= -1 - 2\beta - 2\gamma - \beta\gamma + A'(\gamma\beta + \gamma + \beta) + B' T(\beta + \gamma) + C' \cdot (2\gamma + 1) - D'(2\beta + 1) \\
    h_u(3) &= 2\beta\gamma + \beta + \gamma + A' \beta\gamma + B' T\gamma\beta + C' \gamma + D' \beta \\
    h_u(4) &= \beta\gamma \\
    h_v(1) &= -A'(\beta + \gamma + 1) + B' T + C'(\gamma + 2) - D'(\beta + 2) \\
    h_v(2) &= A'(\gamma\beta + \gamma + \beta) - B' T(\beta + \gamma) + C' \cdot (2\gamma + 1) + D'(2\beta + 1) \\
    h_v(3) &= -A' \gamma + B' T\gamma\beta - C' \gamma - D' \beta
\end{align*}
\]
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   - **Time-domain model**
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Limits of s- and z-domain models

s-domain model
- Relies on the fact that PFD input signal misalignment is sampled so fast that it can be considered a continuous-time operation.
- Might fail for wideband PLLs.
Limits of s- and z-domain models

**s-domain model**
- Relies on the fact that PFD input signal misalignment is sampled so fast that it can be considered a continuous-time operation.
- Might fail for wideband PLLs.

**z-domain model**
- Assumes PFD input signal misalignment is small (pulses $\approx$ impulses).
- Might fail for large frequency jumps.
**CP-PLL time-domain model**

**Classical time-domain simulation limits**

- We need to simulate at least for the settling time (several $T_{\text{ref}}$) while resolving time-steps of fractions of the VCO period.
- Too many simulation steps to resolve output frequency with desired precision.
- Tens-of-hours required.
CP-PLL time-domain model

**Classical time-domain simulation limits**

- We need to simulate at least for the settling time ($T_{ref}$) while resolving time-steps of fractions of the VCO period.
- Too many simulation steps to resolve output frequency with desired precision.
- Tens-of-hours required.

**Better solution**

- Solve state equation describing loop behavior analytically.
- Compute system state variables only on few points per period.
CP-PLL time-domain model

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- Solve state equation describing loop behavior analytically.
- Compute system state variables only on few points per period.
CP-PLL models

Design Example

CP-PLL time-domain model

Next DIV transition found inverting

\[ \int_{t_{\text{inf}}}^{t_{\text{sup}}} f_{\text{out}}(t) \, dt = N \]
Next DIV transition found inverting
\[ \int_{t_{\text{inf}}}^{t_{\text{sup}}} f_{\text{out}}(t) \, dt = N \]

Substituting
\[ \int_{t_{\text{inf}}}^{t_{\text{sup}}} \left( K_{\text{VCO}} \cdot v_c(t) + f_0 \right) \, dt = N \]
Next DIV transition found inverting

\[ \int_{t_{\text{inf}}}^{t_{\text{sup}}} f_{\text{out}}(t) \, dt = N \]

Substituting

\[ \int_{t_{\text{inf}}}^{t_{\text{sup}}} \left( K_{\text{VCO}} \cdot v_c(t) + f_0 \right) \, dt = N \]

Integrating time-independent terms

\[ \int_{t_{\text{inf}}}^{t_{\text{sup}}} v_c(t) \, dt = \frac{N - f_0(t_{\text{sup}} - t_{\text{inf}})}{K_{\text{VCO}}} \]
CP-PLL models

**CP-PLL time-domain model**

**Next DIV transition found inverting**

\[
\int_{t_{\text{inf}}}^{t_{\text{sup}}} f_{\text{out}}(t) dt = N
\]

**Substituting**

\[
\int_{t_{\text{inf}}}^{t_{\text{sup}}} \left( K_{\text{VCO}} \cdot v_c(t) + f_0 \right) dt = N
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**Integrating time-independent terms**

\[
\int_{t_{\text{inf}}}^{t_{\text{sup}}} v_c(t) dt = \frac{N - f_0 \left( t_{\text{sup}} - t_{\text{inf}} \right)}{K_{\text{VCO}}}
\]

**Time-domain solver**

We analytically integrate the term on the left (depending on the 4 cases) and, every \(T_{\text{ref}}\), we numerically invert the obtained equation.
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Estimated settling time for variable $f_{\text{ref}}/f_c$

s-domain vs. time-domain

$f_z = 0.25f_c$, $\tau_0 = T_{\text{ref}}$ (wide frequency jump)

Unreliable for $f_{\text{ref}}/f_c < 10$ (it also fails to predict instability).
Estimated settling time for variable $f_{ref}/f_c$

s-domain vs. time-domain

z-domain vs. time-domain

$f_z = 0.25f_c, \tau_0 = T_{ref}$ (wide frequency jump)

Unreliable for $f_{ref}/f_c < 10$ (it also fails to predict instability).

$f_z = 0.25f_c, \tau_0 = T_{ref}$ (wide frequency jump)

Error can be higher than for s-domain model due to large $\tau_0$ but predicts instability.
Estimated settling time for variable $f_{\text{ref}}/f_c$

s-domain vs. time-domain

z-domain vs. time-domain

$f_z = 0.75f_c$, $\tau_0 = T_{\text{ref}}$ (wide frequency jump)

Higher errors for both models when moving zero from $f_z = 0.25f_c$ to $f_z = 0.75f_c$. 
Estimated settling time
z-domain vs. time-domain

- **z-domain for varying** $\tau_0$, $f_{\text{ref}} \approx 10f_c$
- Error is deeply influenced by first pulse width.
  - For $\tau_0 \to 0$, error always goes to zero.
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Output power spectral density

\[ S_{\theta_o,n} = \| T_R \|^2 S_{\theta_R,n} + \]
\[ + \| T_{PFD} \|^2 S_{\theta_{PFD},n} + \]
\[ + \| T_{CP} \|^2 S_{I_{CP},n} + \]
\[ + \| T_{LF} \|^2 S_{Vc,n} + \]
\[ + \| T_{VCO} \|^2 S_{\theta_{VCO},n} + \]
\[ + \| T_D \|^2 S_{\theta_D,n} \]
Output power spectral density

\[ S_{\theta_{o,n}} = \|T_R\|^2 S_{\theta_{R,n}} + \|T_{PFD}\|^2 S_{\theta_{PFD,n}} + \|T_{CP}\|^2 S_{I_{CP,n}} + \|T_{LF}\|^2 S_{\theta_{VCO,n}} + \|T_D\|^2 S_{\theta_{D,n}} \]

**REF**

\[ T_R = \frac{NG_c(s)}{1 + G_c(s)} \]

**CP**

\[ T_{CP} = \frac{2\pi G_{LF}(s)K_{VCO}}{s(1 + G_c(s))} \]

**DIV**

\[ T_D = -\frac{NG_c(s)}{1 + G_c(s)} \]

**LF**

\[ T_{LF} = \frac{2\pi K_{VCO}}{s(1 + G_c(s))} \]

**PFD**

\[ T_{PFD} = \frac{2\pi G \cdot G_{LF}(s)K_{VCO}}{s(1 + G_c(s))} \]

**VCO**

\[ T_{VCO} = \frac{1}{1 + G_c(s)} \]
s-domain model

\[ T_R = \frac{NG_c(s)}{1 + G_c(s)} \]

\[ T_{CP} = \frac{2\pi G_{LF}(s)K_{VCO}}{s(1 + G_c(s))} \]

\[ T_D = -\frac{NG_c(s)}{1 + G_c(s)} \]

\[ T_{LF} = \frac{2\pi K_{VCO}}{s(1 + G_c(s))} \]

\[ T_{PFD} = \frac{2\pi G \cdot G_{LF}(s)K_{VCO}}{s(1 + G_c(s))} \]

\[ T_{VCO} = \frac{1}{1 + G_c(s)} \]
s-domain model

Output power spectral density

20log(PNoise)

low freq REF noise
(and possibly PFD and CP)

VCO noise

plateau

log f

~fc

\[ T_R = \frac{N G_c(s)}{1 + G_c(s)} \]

\[ T_D = -\frac{N G_c(s)}{1 + G_c(s)} \]

\[ T_{PFD} = \frac{2\pi G \cdot G_{LF}(s) K_{VCO}}{s(1 + G_c(s))} \]

\[ T_{CP} = \frac{2\pi G_{LF}(s) K_{VCO}}{s(1 + G_c(s))} \]

\[ T_{LF} = \frac{2\pi K_{VCO}}{s(1 + G_c(s))} \]

\[ T_{VCO} = \frac{1}{1 + G_c(s)} \]
Time-domain model

- Use time-domain simulator for phase noise analysis
  - Phase noise injected as random jitter which dithers transitions at block outputs.
  - For DIV and REF jitter is added to PFD misalignment.
  - For VCO directly at its output.
  - For the other blocks noise is first converted to jitter at VCO output.
Comparison Examples

- **f_{ref} = 66 MHz**
  - High amount of out-of-band energy folded back.
  - Error taken by s-domain analysis on integrated phase noise is in the order of 80%.

- **f_{ref} = 264 MHz**
  - Error taken by s-domain analysis is in the order of 40% (2^{nd} order) and 20% (4^{th} order).
Comparison Examples

High amount of out-of-band energy folded back. Error taken by s-domain analysis on integrated phase noise is in the order of 80%.

\[ \frac{f_{\text{ref}}}{f_c} \approx 5 \]

Error taken by s-domain analysis is in the order of 40% (2\textsuperscript{nd} order) and 20% (4\textsuperscript{th} order).
Comparison Examples

(a) \( f_{\text{ref}} = 66 \text{ MHz} \)

(b) \( f_{\text{ref}} = 264 \text{ MHz} \)

(c) \( f_{\text{ref}} / f_c \approx 5 \)

High amount of out-of-band energy folded back. Error taken by s-domain analysis on integrated phase noise is in the order of 80%.

(d) \( f_{\text{ref}} / f_c \approx 20 \)

Error taken by s-domain analysis is in the order of 40% (2\textsuperscript{nd} order) and 20% (4\textsuperscript{th} order).
Comparison Examples

2M 10M 100M

\( f_{\text{ref}} = 66 \text{ MHz} \)

\( f_{\text{ref}} = 264 \text{ MHz} \)

\( f_{\text{ref}} = 66 \text{ MHz} \)

\( f_{\text{ref}} = 264 \text{ MHz} \)

\( |\theta_o/\theta_{vco}|^2 \text{ Phase Noise Transfer Function (dB)} \)

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\( |\theta_o/\theta_{vco}|^2 \text{ Phase Noise Transfer Function (dB)} \)

High amount of out-of-band energy folded back. Error taken by s-domain analysis on integrated phase noise is in the order of 80%.

Error taken by s-domain analysis is in the order of 40% (2\(^{\text{nd}}\) order) and 20% (4\(^{\text{th}}\) order).
s-domain model can become unreliable if $f_{ref}/f_c < 20$.
Even z-domain model fails for large frequency jumps.
Results

Models comparison

- s-domain model can become unreliable if \( \frac{f_{\text{ref}}}{f_c} < 20 \).
- Even z-domain model fails for large frequency jumps.
- Time-domain model can be used to efficiently simulate wideband PLLs
  - Fast enough to be extensively used.
  - It can be easily extended to perform averaged analysis of phase noise.
  - Model has been validated designing a frequency synthesizer for UWB MB-OFDM.
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**Federal Communication Commission**

- FCC authorizes use of 3.1-to-10.6GHz spectrum.
- Bandwidth larger than 500MHz.
- Power spectral density of emission below -41.3 dBm/Hz.
# UWB communications

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Mb/s</td>
<td>1 km</td>
</tr>
<tr>
<td>1 Gb/s</td>
<td>10 km</td>
</tr>
<tr>
<td>100 Mb/s</td>
<td>100 km</td>
</tr>
</tbody>
</table>

## Federal Communication Commission
- FCC authorizes use of 3.1-to-10.6GHz spectrum.
- Bandwidth larger than 500MHz.
- Power spectral density of emission below -41.3 dBm/Hz.

## Target applications
- Low range (<10m).
- High data rates (>100Mb/sec).
UWB communications

Target applications

- Low range (<10m).
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UWB communications

Target applications

- Low range (<10m).
- High data rates (>100Mb/sec).
- Personal Area Networks.
WiMedia Alliance Proposal

- ECMA standards 368 and 369.
- Data rates up to 480 Mb/sec.
- QPSK or DCM modulation schemes.
### WiMedia Alliance Proposal

- ECMA standards 368 and 369.
- Data rates up to 480 Mb/sec.
- QPSK or DCM modulation schemes.

<table>
<thead>
<tr>
<th>Group 1</th>
<th>Group 2</th>
<th>Group 4</th>
<th>Group 3</th>
<th>Group 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avoid</td>
<td>Detect</td>
<td>Available</td>
<td>Not available</td>
<td>Available</td>
</tr>
<tr>
<td>10296</td>
<td>9768</td>
<td>8712</td>
<td>8184</td>
<td>7656</td>
</tr>
<tr>
<td>3960</td>
<td>7128</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ECMA standard

- 14 bands organized in 6 band groups.
- MultiBand Orthogonal Frequency Division Multiplexing (MB-OFDM).
- Different subsets of frequencies allowed outside US.
**UWB MB-OFDM**

<table>
<thead>
<tr>
<th>CENTER FREQ IN MHz</th>
<th>GROUP 1</th>
<th>GROUP 2</th>
<th>GROUP 3</th>
<th>GROUP 4</th>
<th>GROUP 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>USA</td>
<td>3432</td>
<td>3960</td>
<td>5016</td>
<td>6072</td>
<td>6600</td>
</tr>
<tr>
<td>EUROPE</td>
<td>5544</td>
<td>6600</td>
<td>7128</td>
<td>7656</td>
<td>8184</td>
</tr>
<tr>
<td>JAPAN</td>
<td>9240</td>
<td>8712</td>
<td>9768</td>
<td>10296</td>
<td></td>
</tr>
<tr>
<td>KOREA</td>
<td>10296</td>
<td>8712</td>
<td>9768</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **ECMA standard**
  - 14 bands organized in 6 band groups.
  - MultiBand Orthogonal Frequency Division Multiplexing (MB-OFDM).
  - Different subsets of frequencies allowed outside US.
**ECMA standard**

- OFDM symbol last 242.42ns plus 70.08ns for zero-padded suffix.
- Switching between bands every 312.5ns.
- 9.5ns of guard interval.
UWB MB-OFDM Transceiver
Outline

1 CP-PLL models
   - The need for accurate PLL models
   - s-domain model
   - z-domain model
   - Time-domain model
   - Comparison between models
   - Phase Noise Models

2 Design Example: Frequency Synthesizer for UWB MB-OFDM
   - UWB communications
   - Synthesizer Architecture
   - PLLs
   - Tuning Range Extension
   - Measured results
Target Specifications

System specifications

- Frequency range: 3432-to-10296MHz.
- 14 center frequencies to be synthesized.
- Integrated Phase noise below $3.6^{\circ}_{\text{RMS}}$.
- Aggregate power of spurs lower than -24dBc.
- Frequency switching time (for bands in the same group) lower than 9.5ns.
**Architecture**

**Classic solutions**

- Multiple fixed-frequency PLLs not suitable for full spectrum coverage.
**Classic solutions**

- Multiple fixed-frequency PLLs not suitable for full spectrum coverage.
- State-of-the-art solutions generally make use of fixed frequency PLLs and extensive mixing.
  - Area overhead due to the presence of inductors for band-pass filtering.
  - High power consumption.

**Architecture**

Diagram showing the architecture of the CP-PLL models with multiple fixed-frequency PLLs and extensive mixing circuits.

Diagram showing the proposed solution with two PLLs synthesizing frequencies in the 6.6-to-10.3GHz range and two circuits extending the tuning range down to 3.4GHz. MUX switches between the two output every 312.5ns.
**Architecture**

- **TCXO 66 MHz**
- **IC**
  - **Wideband PLL**
  - **TREC**
  - **MUX**
  - **CONTROL**

**Proposed solution**

- Two PLLs synthesize frequencies in the 6.6-to-10.3GHz range.
- Two circuits extend the tuning range down to 3.4GHz.
- MUX switches between the two output every 312.5ns.
Outline

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PLL high level design and simulations

Loop design

- Fourth-order loop.
- Open-loop unit gain frequency 8MHz.
- Reference frequency of 66MHz.
PLL high level design and simulations

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### Design Example

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{ref}$</td>
<td>66MHz</td>
</tr>
<tr>
<td>$I_{CP}$</td>
<td>200-400 μA</td>
</tr>
<tr>
<td>$K_{VCO}$</td>
<td>≈600 to 2000MHz/V</td>
</tr>
<tr>
<td>$N$</td>
<td>100-156</td>
</tr>
<tr>
<td>$f_c$</td>
<td>8MHz</td>
</tr>
<tr>
<td>$f_p$</td>
<td>30 and 60MHz</td>
</tr>
</tbody>
</table>
Outline

1. CP-PLL models
   - The need for accurate PLL models
   - s-domain model
   - z-domain model
   - Time-domain model
   - Comparison between models
   - Phase Noise Models

2. Design Example: Frequency Synthesizer for UWB MB-OFDM
   - UWB communications
   - Synthesizer Architecture
   - PLLs
   - Tuning Range Extension
   - Measured results
Tuning Range Extension Circuit

\[ F_{out} = \frac{F_{vco}}{DIV} \]
Tuning Range Extension Circuit

\[ F_{\text{out}} = \frac{F_{\text{VCO}}}{\text{DIV}} \]

<table>
<thead>
<tr>
<th>( F_{\text{OUT}} \text{ (MHz)} )</th>
<th>( \text{DIV} )</th>
<th>( S_0 )</th>
<th>( S_1 )</th>
<th>( F_{\text{VCO}} \text{ (MHz)} )</th>
<th>( F_1 \text{ (MHz)} )</th>
<th>( F_2 \text{ (MHz)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>3432</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>6864</td>
<td>6864</td>
<td>3432</td>
</tr>
<tr>
<td>3960</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>7920</td>
<td>7920</td>
<td>3960</td>
</tr>
<tr>
<td>4488</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>8976</td>
<td>8976</td>
<td>4488</td>
</tr>
</tbody>
</table>
Tuning Range Extension Circuit

\[ F_{\text{OUT}}(\text{MHz}) \quad \text{DIV} \quad S_0 \quad S_1 \quad F_{\text{VCO}}(\text{MHz}) \quad F_1(\text{MHz}) \quad F_2(\text{MHz}) \\
3432 \quad 2 \quad 1 \quad 0 \quad 6864 \quad 6864 \quad 3432 \\
3960 \quad 2 \quad 1 \quad 0 \quad 7920 \quad 7920 \quad 3960 \\
4488 \quad 2 \quad 1 \quad 0 \quad 8976 \quad 8976 \quad 4488 \\
5016 \quad 1.5 \quad 0 \quad 0 \quad 7524 \quad 5016 \quad 2508 \\
5544 \quad 1.5 \quad 0 \quad 0 \quad 8316 \quad 5544 \quad 2772 \\
6072 \quad 1.5 \quad 0 \quad 0 \quad 9108 \quad 6072 \quad 3036 \]
Tuning Range Extension Circuit

![Diagram of tuning range extension circuit](image)

<table>
<thead>
<tr>
<th>$F_{OUT}$(MHz)</th>
<th>DIV</th>
<th>$S_0 S_1$</th>
<th>$F_{VCO}$(MHz)</th>
<th>$F_1$(MHz)</th>
<th>$F_2$(MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3432</td>
<td>2</td>
<td>1 0</td>
<td>6864</td>
<td>6864</td>
<td>3432</td>
</tr>
<tr>
<td>3960</td>
<td>2</td>
<td>1 0</td>
<td>7920</td>
<td>7920</td>
<td>3960</td>
</tr>
<tr>
<td>4488</td>
<td>2</td>
<td>1 0</td>
<td>8976</td>
<td>8976</td>
<td>4488</td>
</tr>
<tr>
<td>5016</td>
<td>1.5</td>
<td>0 0</td>
<td>7524</td>
<td>5016</td>
<td>2508</td>
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<tr>
<td>5544</td>
<td>1.5</td>
<td>0 0</td>
<td>8316</td>
<td>5544</td>
<td>2772</td>
</tr>
<tr>
<td>6072</td>
<td>1.5</td>
<td>0 0</td>
<td>9108</td>
<td>6072</td>
<td>3036</td>
</tr>
<tr>
<td>6600-10296</td>
<td>1</td>
<td>X 1</td>
<td>6600-10296</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Outline

1 CP-PLL models
   - The need for accurate PLL models
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Test chip

Die

- TSMC 90nm CMOS process.
- Die area 2x2mm$^2$.
- Core area 0.5mm$^2$. 
Test chip

Die

- TSMC 90nm CMOS process.
- Die area 2x2mm$^2$.
- Core area 0.5mm$^2$.

<table>
<thead>
<tr>
<th>Component</th>
<th>Area (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>QVCOs</td>
<td>85%</td>
</tr>
<tr>
<td>Loop filters</td>
<td>12%</td>
</tr>
<tr>
<td>Charge Pumps</td>
<td>1.5%</td>
</tr>
<tr>
<td>TREC$^*$s</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>Dividers</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>PFDs</td>
<td>&lt;1%</td>
</tr>
</tbody>
</table>
Output spectra (3.4-9.2GHz range)

Band 1 (TREC divides by 2).

Output Spectra of the synthesizer
Output spectra (3.4-9.2GHz range)

Output Spectra of the synthesizer

- Band 1 (TREC divides by 2).
- Band 4 (TREC divides by 1.5).
Output spectra (3.4-9.2GHz range)

Output Spectra of the synthesizer
- Band 1 (TREC divides by 2).
- Band 4 (TREC divides by 1.5).
- Band 7 (TREC acts as buffer).
Output spectra (3.4-9.2GHz range)

- Band 1 (TREC divides by 2).
- Band 4 (TREC divides by 1.5).
- Band 7 (TREC acts as buffer).
- Highest spur is at -32dBc.
Output spectra (3.4-9.2GHz range)

Output Spectra of the synthesizer

- Highest reference spur at -39dBc.
- Aggregate spur power -27dBc.
- Specifications require -24dBc.
Phase Noise

- Spectrum close-in (1MHz wide).
  - Phase noise -107dBc/Hz at 50KHz.
  - Phase noise -110dBc/Hz at 100KHz.
  - Some spurs due to digital noise.
Phase Noise

Spectrum close-in (1MHz wide).
- Phase noise -107dBc/Hz at 50KHz.
- Phase noise -110dBc/Hz at 100KHz.
- Some spurs due to digital noise.

Integrated Phase noise.
- \( 1.1^{\circ}_{RMS} \) at 3432MHz.
- \( 2.8^{\circ}_{RMS} \) at 9240MHz.
- Estimated \( 3.1^{\circ}_{RMS} \) at 10296MHz.
- Specification \( 3.6^{\circ}_{RMS} \).
Frequency switching behavior

VCOs control voltages
- First PLL settles in $T_a$.
- Second PLL settles in $T_b$.
Frequency switching behavior

VCOs control voltages

- First PLL settles in $T_a$.
- Second PLL settles in $T_b$.
- Simulated data points are minimum and maximum values for each reference period.
- Filtering effect due to capacitive load on control voltages buffers.
- Settling time estimated to be below 300ns.
Results and comparison with previous solutions

<table>
<thead>
<tr>
<th></th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>180nm CMOS</td>
<td>180nm CMOS</td>
<td>180nm CMOS</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>$V_{supply}$</td>
<td>1.8V</td>
<td>1.8V</td>
<td>1.8V</td>
<td>1.2/1.8V</td>
</tr>
<tr>
<td>$F_{out}$</td>
<td>3432-10296 MHz</td>
<td>3432-10296 MHz</td>
<td>6336-8976 MHz</td>
<td>3432-9240 MHz</td>
</tr>
<tr>
<td>$F_{ref}$</td>
<td>264MHz</td>
<td>66MHz</td>
<td>528MHz</td>
<td>66MHz</td>
</tr>
<tr>
<td>Phase noise</td>
<td>-98dBc/Hz @1MHz</td>
<td>-</td>
<td>-109.6dBc/Hz @1MHz</td>
<td>-99dBc/Hz @100KHz</td>
</tr>
<tr>
<td>Spurs</td>
<td>-33dBc</td>
<td>-35dBc</td>
<td>-52dBc</td>
<td>-32dBc</td>
</tr>
<tr>
<td>Power</td>
<td>117mW</td>
<td>162mW</td>
<td>58mW</td>
<td>55mW</td>
</tr>
<tr>
<td>Area</td>
<td>2.5x2.2$mm^2$ (full chip)</td>
<td>1.2x1.3$mm^2$ (core)</td>
<td>0.7x1.1$mm^2$ (single PLL core)</td>
<td>0.5$mm^2$ (core)</td>
</tr>
</tbody>
</table>

Comparison

Joint power consumption and area occupation are better than state-of-the-art solutions.

1 Che-Fu Liang et al., ISSCC2006.
3 Geum-Young Tak et al., JSSCC2005.