Frequency synthesizers for RF transceivers

- Introduction
  - Frequency synthesizer requirements for integrated RF transceivers
  - Phase locked-loops (PLL): architecture, and working principle and building blocks
- PLL Modeling
  - Modeling of PLL in the frequency and time domain
  - Noise in PLLs
- Design examples:
  1) Synthesizer for UWB receivers (integer-N PLL)
  2) Synthesizer and VCOs for fully-integrated reconfigurable multi-standard transceivers:
     - high tuning-range VCO
     - fractional-N synthesizers with techniques for spurious compensation and increased linearity.
Introduction

- Wireless and cellular standards require low-cost, low-power
- Sub-micron CMOS technologies achieve:
  - High transistor cut-off frequencies
  - "Low cost" technologies
  - VLSI for digital signal processing

RF front-end transceiver and the base band processor can be realized on the same chip.

**RF front-end of direct conversion transceiver**

- Zero-IF receiver
- Direct-up transmitter
Frequency synthesizer requirements

- **tuning range** i.e. capability of synthesizing various RF frequencies according to the transceiver architecture and the communication system (channel spacing)
- **frequency accuracy** and stability in time and temperature
- **spectral purity**: phase noise and spurs
- **switching time**

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Phase Noise

- Due to the noise of the electronic circuits the oscillator outputs can be written as $V_{\text{out}} = A(t) \cos(\omega_0 t + \phi(t))$
- Phase noise:
  $$L(\Delta\omega) = 10 \log_{10} \left( \frac{\text{Noise in a 1Hz band at } \omega_0 + \Delta\omega}{\text{Carrier power}} \right)$$

- **FOM**:
  $$FOM = -L(\Delta\omega) + 10 \log \left( \frac{\omega_0}{\Delta\omega} \right)^2 \cdot \frac{1}{P}$$
Effect of phase-noise in a receiver

From RF Microelectronics Razavi, 1998, Fig. 7.13

Effect of spurs in a receiver

From RF Microelectronics Razavi, 1998, Fig. 8.2
Characteristics of some communication standards and phase noise requirements

- **DECT**
  - 10 channels spaced of 1.728 MHz from 1881 to 1897 MHz
  - Settling time < 400 µs
  - Phase Noise < -114 dBC/Hz @ 5.184MHz

- **UWB MB-OFDM**
  - Frequency range: 3432-to-10296 MHz.
  - 14 center frequencies to be synthesized, spaced of 528 MHz
  - Frequency switching time lower than 9.5 ns
  - Accuracy 20 ppm
  - Integrated Phase noise below 3.6° RMS
  - Aggregate power of spurs lower than -24 dBc

- **UMTS RX**
  - Tuning range 60 MHz (2110 to 2170 MHz)
  - channel spacing 5 MHz
  - Phase Noise -130 dBC/Hz @1MHz

- **E-GSM RX**
  - Tuning range 35 MHz (925 to 960 MHz)
  - channel spacing 200 kHz
  - Phase Noise -141 dBC/Hz @3MHz

- **IEEE 802.11b (WLAN)**
  - Tuning range 84 MHz (2400 to 2483.5 MHz)
  - Channel spacing 20 MHz
  - Phase Noise -107 dBC/Hz @1MHz
**Integer-N PLL (Charge Pump Phase-Locked Loop)**

- Phase Frequency Detector (PFD)
- Charge Pump (CP)
- Low Pass Filter (LPF)
- Voltage Controlled Oscillator (VCO)
- Frequency Divider (FD)

![PLL Diagram]

\[ \text{Fout} = \text{Fref} \times N \]

**Voltage Controlled Oscillator (VCO)**

- LC oscillator
- Large area (integrated inductors)
- Fine tuning obtained by variable capacitor \( C = C(V_c) \) (varactor)
- Coarse tuning through array of switchable capacitors

\[ f_o = \frac{1}{2\pi \sqrt{LC}} \]

\[ C = C_{\text{fixed}} + C_{\text{programmable}} \]
\[ \omega_{\text{out}} = \omega_{\text{FR}} + K_{\text{VCO}} V_C \quad K_{\text{VCO}} = \frac{d\omega}{dV_c} \]
**Frequency divider (FD)**

\[ F_{\text{OUT}} \xrightarrow{FD} F_{\text{DIV}} = \frac{F_{\text{OUT}}}{N} \]

- \( F_{\text{OUT}} \) in the GHz range
- \( F_{\text{ref}} \) in the MHz range
- \( N \) in the order of \( 10^2 \)
- change in output frequency achieved by changing \( N \)

**Programmable divider**

Dual Modulus Prescaler

\[ N = (N_p + 1)S + N_p(P-S) = P \cdot N_p + S \]

with \( P > S \) and \( S_{\text{max}} = N_p-1 \)

Es: \( N_p = 4, S = 0..3, P = 0..31 \)

\( N_{\text{max}} = 127, N_{\text{min}} = 16 \)

assuming \( F_{\text{REF}} = 66 \text{ MHz}, F_{\text{OUT}} = 1056 - 8382 \text{ MHz} \)
Dual Modulus Prescaler (DMP)

MOD = 1  \( F_{\text{out}} = \frac{1}{5} F_{\text{input}} \)
MOD = 0  \( F_{\text{out}} = \frac{1}{4} F_{\text{input}} \)

Counters

• synchronous:
  – high load capacitance
  – high power consumption

• asynchronous
  – add delay between input and output
**Phase Frequency Detector (PFD) and Charge-Pump (CP)**

Converts phase misalignment between ref and div into current pulses of variable width

\[ Q_c = \frac{\Delta \theta}{2\pi} GT \]

**Loop Filter**

Integrates error signal and converts the CP current pulses into the VCO control voltage

Es: second order loop filter
   high order filter can be convenient to remove out-of-band noise
Frequency synthesis with integer-N PLL

Example: frequency synthesizer for UWB

F_{\text{VCO}} \rightarrow \frac{1}{2} \rightarrow \text{DMP} \rightarrow \text{Prop. Control} \rightarrow \text{F}_{\text{ref}}

Switching signal instant

N=52 \times 2

N=78 \times 2

F_{\text{ref}} = 66 \text{ MHz}
Reference frequency and integer-N PLL

- Trade-off between channel spacing and switching time
  - $F_{\text{out}}$ is an integer multiple of $F_{\text{ref}}$
  - $F_{\text{ref}}$ must be equal to channel spacing (i.e. 200 kHz in GSM)
  - stability requirements limit the closed-loop bandwidth to roughly $(1/10) F_{\text{ref}}$
  - $F_{\text{ref}}$ must be high to reduce the switching time

  Fractional-N divider to overcome this problem

Bibliography

2. RF Microelectronics, B. Razavi, Prentice-Hall, 1998